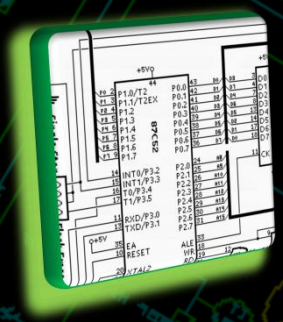
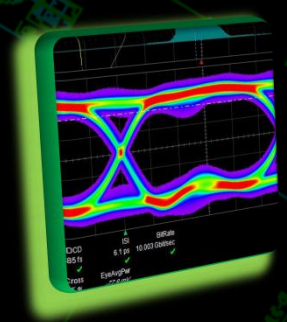
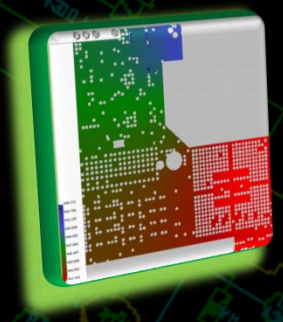
Electronic Design Verification



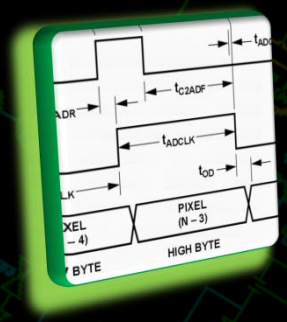
Schematic Integrity™



Signal Integrity



Power Integrity



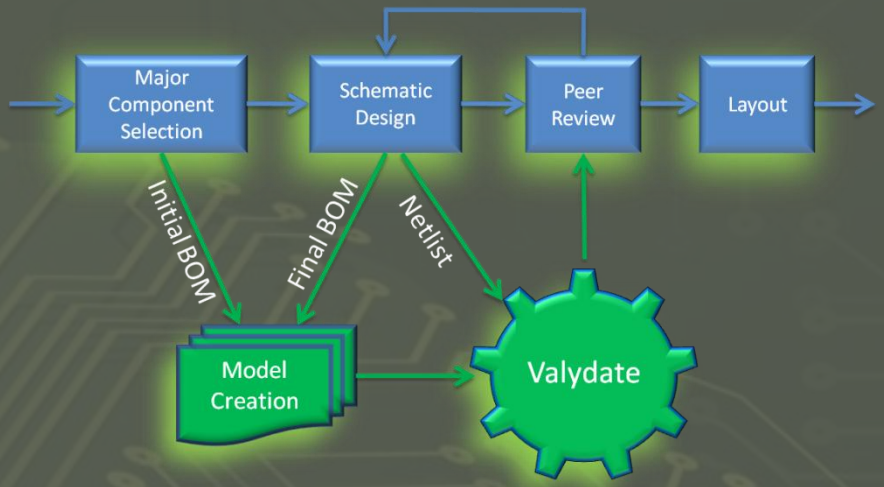
Static Timing

Valydate

Schematic Integrity Analysis™

Schematic designs are far too complex to thoroughly inspect using human-peer-review techniques. The implications of defects escaping at this stage of design are profound, and include excessive consumption of scarce engineering talent to debug problems, lengthy NPI delays, poor production yields, high in-warranty costs and degradation of customer satisfaction.

Valydate saves design teams hundreds of hours of visual inspection and lab debug time by automating **> 70 proprietary checks** for each net within the emerging design. These checks (examples listed on the right) execute rapidly and immediately prior to your schematic freeze milestone, such that layout may commence with highest confidence of 1st pass success.



Valydate's Schematic Integrity Analysis is performed in parallel with your design and does not affect the schedule of your hardware development (Except for saving you time during lab testing and debugging!).

Examples of the hundreds of thousands of checks performed

- Pin Parametric Verification for max, min and logic thresholds
- Bus flip errors (MSB to LSB, TX and RX errors)
- Full Multi Board and Backplane interface Verification
- Pin Function compatibility tests
- Symbol mismatch to datasheet
- Driver/Receiver Technology Matching
- Diode orientation verification
- Driver/Receiver Function Matching
- Power/Ground/Open Collector/Drain shorts
- Capacitor decoupling sufficiency checks
- Capacitor Voltage De-rating (to client rules)
- Redundant resistors on a net detection
- Open collector/Drain verification
- Poor design practice checks (ie: using pull-ups, pull downs when needed...)
- Power/Ground plane connection verification
- Component power checks
- Multiple or missing power supplies on a net
- Differential Pin Verification
- Unconnected nets or bus detection
- Off-board nets detection
- Overloaded pins identification
- Unconnected mandatory pins identification
- Nets missing driver
- Nets missing receiver
- And many more…

Our Clients

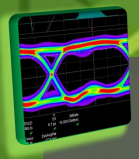
Alcatel·Lucent

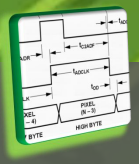
GENERAL DYNAMICS

"A *must have* process before fabrication to avoid unnecessary re-spin"
VP of Digital Hardware Eng.,
ATE Solutions Provider

ciena

CURTISS WRIGHT Controls Embedded Computing



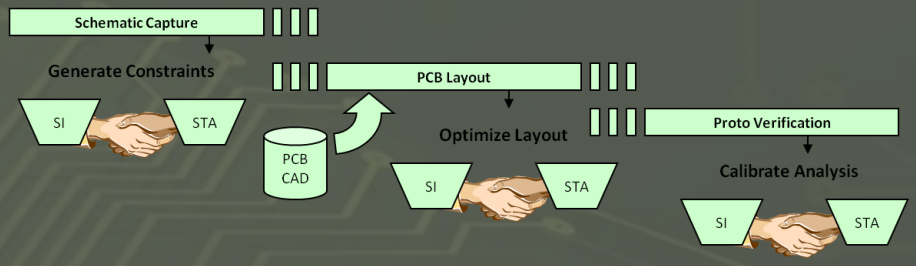


Signal Integrity & Static Timing Analysis

Today's high speed designs and escalating complexity require detailed, integrated analytic attention to assure Signal Integrity and Inter-Device Timing match product environmental performance needs. Such attention produces lower electromagnetic emissions, higher manufacturing yield, superior in-field reliability and marked improvements in Time-to-Market.

Valydate provides the thorough analysis world-class products require, enhancing your internal design process with expert intervention to maximize first-pass layout success rate. The result is optimized Signal Quality and Timing Margins on each performance-critical net in your design.

From initial layout constraints generation through layout to prototype validation, let Valydate's experienced staff and world-class tools guide you to systemically improved design productivity and business success.



Valydate's Integrated approach is specifically designed to maximize the compatibility of your product's performance with its operating environment. Application early in your process will assure a clean 1st pass design.

Thorough Pre-layout Constraints Generation

- Stackup analysis defines optimal materials, layer definitions, routing technology, and grounding scheme.
- Manhattan-based Signal Quality constraints generation
- Trace length constraints and mathematical trace relationship constraints
- Drive strength optimization

Precise Post-Layout Optimization

- Comprehensive re-check of actual layout to assure preservation of Signal Quality and Static Timing
- Actual track lengths are back-annotated into timing analysis
- Recommendations for layout adjustments to center timing and maximize margins

Precise constraints maximize 1st pass Success…

…and live with the product through its life

Our Clients

matrox

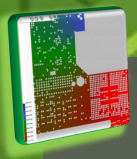
sandvine
Intelligent Broadband Networks

"Valydate's analysis service identified real errors before we committed our design. This helped us get to market faster with a higher quality product."

Ben Brown
VP Engineering, LTX-Credence

CHRISTIE

COMMSCOPE



Power Integrity Analysis

Modern electronic designs employ-increasing IC density, distributed power architectures, use of dozens of board voltages, increasing count of PCB layout planes, high technology stackups and fine-pitch componentry.

Failure to assure adequate power delivery to each device on a design can result in Signal Integrity degradations up to and including the total failure of the design's functionality.

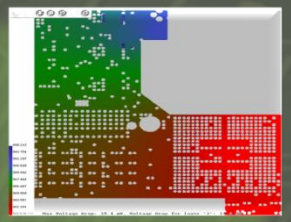
To assure the seamless design of a clean power system, board designers need to identify and solve complex distribution problems early in their design cycle.

The application of Valydate's Power Integrity Analysis assures that:

- Power distribution issues are highlighted prior to layout freeze
- Quantified noise levels are visible on a part-by part level
- 'What-if' solution alternatives are explored and decided
- Confidence is achieved prior to artwork-commit

IR Drop

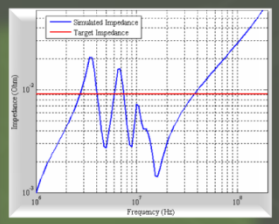
Valydate's Power Integrity Analysis comprehensively identifies all areas of IR Drop concern, and provides specific implementation guidance for available solutions



- Excessive IR voltage drop on tracks
- Areas of excessive current density
- Via current density
- Ground and power plane optimization
- Visualize noise environment

Power Distribution Analysis (PDR)

Power Integrity Analysis optimizes your decoupling scheme, stack up, ground / power plane design and via count/placement



- Optimize on-board impedances
- Add/ remove/change/replace decoupling caps
- Modify routing/pads/stackup
- Modify stitching
- Visualize noise environment
- Extraction of accurate via models for multi-gigahertz SI analysis

Our Clients

Haivision NETWORK VIDEO

FLEXTRONICS

"Valydate's Schematic Integrity service has been very useful; not only in finding some issues, but also as a thorough check in verifying that other parts of the design have been done correctly."

Milan Fait
Alcatel-Lucent HW Design

kontron

VISUALSONICS

Corporate Headquarters
308 Legget Drive
Suite 200
Ottawa, Ontario, K2K 1Y6
Canada

valydate

Tel: 1 613 627 4702
Email: info@valydate.com
www.valydate.com