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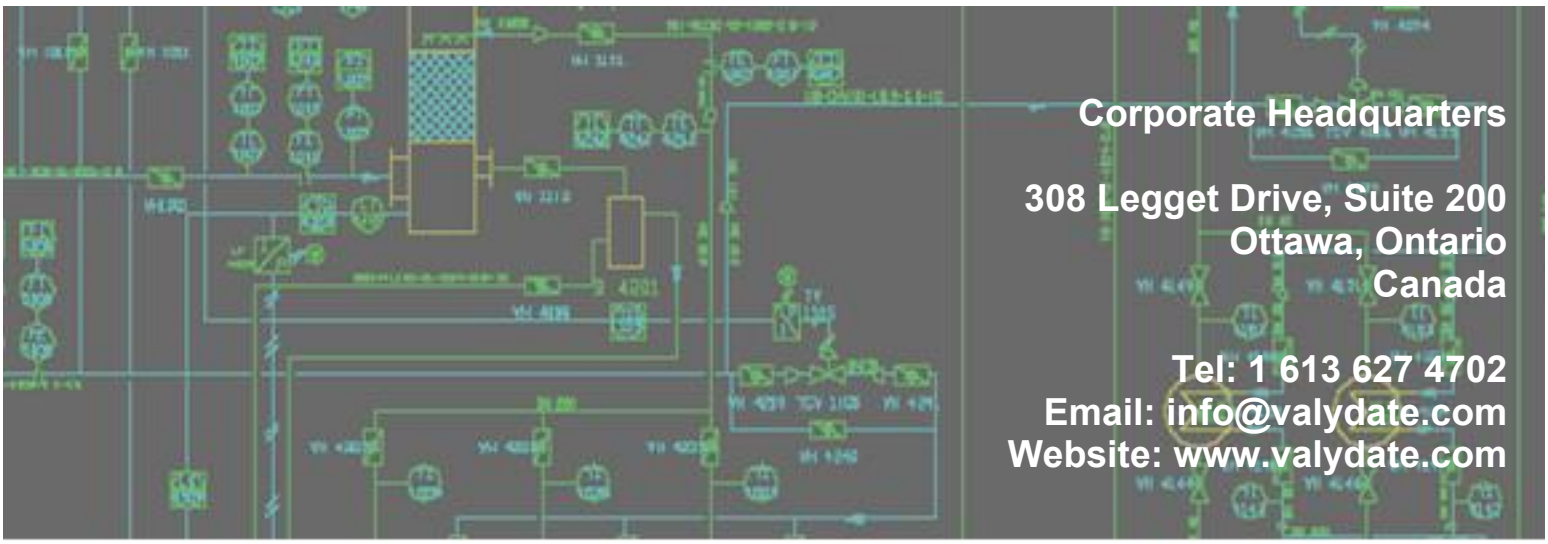
Schematic Analysis Report

Project Name :	**Example**
Company Name :	**Valydate Inc.**
Report Number :	**13-1-Valydate-R1**
PO Number :	**N/A**
Prepared For :	**Peter Campbell**
Report Date :	**Jun-26-13**



Executive Summary

Valydate Inc. requested that Valydate perform a Schematic Integrity Analysis on Example. The objective of the verification was to identify design defects and marginalities (at the schematic level) and to recommend solutions. An additional objective is to highlight other design improvement opportunities and solutions compatible with good design practice.

This report details the results of the Valydate Inc. Schematic file 'Specifies exact filename and date' as received from Valydate Inc..

This is an example report to illustrate format and nature of findings Valydate creates.

Product Metrics :

Number of Nets verified : **2500**

Total count of devices : **2700**

Total findings from Valydate Analysis : **51**

Analysis Outcome - Severity : Qty

Critical Defect : **18** A defect that will (or is highly likely to) cause damage to or functional disruption of the client's product. Such defects will require action on both the schematic and its related PCB artwork.

Defects + Warnings : **33** A defect that could cause damage, degradation of operating lifetime or intermittent functional disruption of the client's product, if the product is subjected to corner-case production variation or environmental exposure, or

An observation and/or recommendation which improves robustness or utility of the design, or aids in its manufacturability/testability/re-use.

These items are known to not cause product field failure and represent an opportunity for improvement.

Valydate suggests that a follow-up teleconference be held during the week of 26/06/2013 to review these findings to assure clarity of recommendations herein, and to obtain Valydate Inc.'s feedback on the value of the analysis results delivered.

Design Files Used in Valydate Analysis :

Schematic Version :	**Specifies exact filename and date**
BoM Version :	**Specifies exact filename and date**
Netlist Version :	**Specifies exact filename and date**

Records :

The necessary records obtained or created during this verification will be maintained for a period of a minimum of 3 months in case Valydate Inc. would like to re-run this analysis after changes are performed on the Example.

Conflict of Interest :

The lead verifier and the verification team is/are independent from the project, project proponent(s), quantifier, and/or any agent related to the project. The Valydate team maintained objectivity throughout the verification to ensure that the findings and conclusions are based on objective findings generated during the verification.

Verification Methodology :

Valydate uses the ValydateDesign© toolset to identify defects and marginalities within product schematic designs. This automated tool checks each digital net on the schematic, applying over 50 proprietary checks. The steps performed are outlined below:

1. Valydate receives a BoM, netlist, .pdf schematic and ancilliary files from customer
2. The BoM and Netlist are loaded into the Valydate analysis environment.
3. The BOM and Netlist are consolidated and ValydateDesign© is run on the design, producing itemized results.
4. The results are analyzed by Valydate engineering staff, producing design change recommendations classified as Critical Defects, Defects or Warnings
5. After any design corrections are completed, the analysis is re-run on fresh design files to assure the revised schematic is 100% verified, and no new violations have been created.

Detailed Findings :

This section itemizes the detailed findings of the analysis, listing known and suspected defects, their implications and suggested corrective action

Critical Defects : 18

#	Defect Description Comments
C 1	Bus significance does not match on net $24N46 at U39-AF21 (on xxx) and U15-C23 Unsure the FPGA is aware of the PPC Endianess difference. Please ensure that the FPGA is aware that A31 is LSB.
C 2	Differential net pair GXB_RX_3_P and GXB_RX_3_N cross wired.(Ref. J1-226) Please check intent on J1-226 and -228. U1 is programmed for these connections to be the reverse of what is written on the schematic on page 2.
C 3	The supplied netlist does not have GNDD pins as with previous analysis. Please see “Untested Nets.doc” – Section 4 for the listing. Valydate strongly recommends adding these missing GNDD connections to schematic
C 4	More than 1 differential input on net 15N5224 at U6-J12 (on xxxx) U6-H12 (on xxxx) U6-AD12 (on xxxx) U6-AC12 (on xxxx) Biasing the ECL with the capacitor is ok for AC but not for DC biasing.
C 5	2 sets of differential pairs on net XFI-OTN_02_RD- at U17-AE39(Main) U19-P1(Daughter) Input to input
C 6	More than 1 output on net DEV_WE_N2 at U18-D3 and U26-M8 U18 pin D3 and U26 pin M8 are both defined as output pins. (U18 defines tri-out,U26 defines tri-out). Schematic says U26 pin M8 = INPUT.
C 7	More than 1 output on net PCI_RESET_L at J6-D40 ,U49-N27 This is a driven output from the FPGA. This signal is supposed to be an open drain.
C 8	More than 1 output on net PDB_TDO at U62-3 and U62-6 Absent of the xxx card, net JTAG_EMU_ISOL_N is pulled high, disabling Y2 output of U62. Issue exists if yyy card drives this net low in contention with
C 9	Differential output with no input on net 155.52_MHZ_OUT_N;P at U116-T8;R8 Xilinx FPGA must define these pins.
C 10	Ground pins detected at U86-8, with no ground source on net CLOCK N$42760 Datasheet does not indicate that these pins are different from other 2 ground pins. Please connect them to GND.
C 11	Ground pins detected at U80-3 , with no ground source on net DGND DGND is not connected to any other GND
C 12	No Open Collector Drain inputs on net $40N479. Pins U69-5 An external pullup for this circuit is required to work.
C 13	4 occurrences of power pins detected with no power source on net +1.2VDD_YA_ISO_VDD12_SX2 at refdes U96-T7 This net is pulled to ground. Reconnect to appropriate power source
C 14	Pull down R375 for pin is not correctly connected. For the PPC405 to function the TRST pin must be held low for normal operation, but is pulled high by R8.
C 15	Pull down R375 for pin is not connected to voltage rail. For the PPC405 to function the TRST pin must be held low for normal operation, but is pulled high by R8.
C 16	Input U6-P4 has built in pull down of 9.0K. Please check that refdes R237 is sufficient to ensure proper thresholds R237 is not strong enough to overcome internal pull down. (9k internal pulldown per Altera Schematic Review Worksheet)
C 17	Pin functions do not match between U1P23-9(pin name SCL) and U11P30-6(pin name SDA) SDA and CLK pins swapped on U11P30
C 18	Driver pin 9 (pin PWM2) of U275 has lower Vout Max (3.39V) than rcvr Vinh pin 40 (pin PWM) of U276 (4.2V) on net N67604281 The output of the PV3012 will drive a 3.3V logic signal while the SIC769 requires a 5V logic signal.

Defects : 17

#	Defect Description Comments
D 1	All inputs on net FPGA_SEL_PROT_IF ,U96-J18 This signal is not connected to anything.
D 2	All inputs on net BPX_RSTACT_N ,U17-E16 , U26-E12 These are inputs that are connected to the backplane. There are no pullups/downs on the net even down to the motherboard.
D 3	All inputs on net QSFP_PHY2_NVMA1SEL ,U64-J4 As a good design practice an external pull up should be added.
D 4	All inputs on net N844686319 ,U50-H1 (on xxx), Consider an external pulldown to assure full duplex operation
D 5	Differential net pair 167M_N and 167M_P cross wired. Cross wired diff pair clock. While it’s not a problem it may be confusing.
D 6	Banks 3A and 3B on FPGA are powered by 1.5V which will not be suitable for driving LVDS-25 signals Expected 2.5V
D 7	No Connect pin connected to net $6N884 – U7-D6 CPU_PLD_JTAG_EN_L is not implemented on the Lattice FPGA
D 8	No Connect pin connected to net T41-T41_XFI3_TX_FILTP - U50-N39 The datasheet has these as an NC. Note that the P/N nets are swapped
D 9	Too many pull ups for Open Collector Drain net UCD_ALERT_N (R31, R101) Please remove extra pullup
	Net VREF_KBP Vmax (0.918V) is greater than allowable Vmax (0.85V) on refdes U20 pin G3

10	The datasheet for the NL7512 show that these pins need a VREF of .68 to .85 for HSTL.
D	Driver on refdes U17-57 (pin name PR7B) has higher Vout Max (3.399V) than receiver Vin Max on refdes U11pins E1,E3,E24,E26 (pin names RESET
11	The LCMXO256 is powered from 3.3V while the BCM84834 pin is powered from 2.5V
D	Driver on U8-N10 (pin PB23B) has higher Vout Max (3.399V) than receiver Vin Max on U118-P33 (pin ALTERA_DATA7_RESERVED_INPUT)(2.575V) on
12	While the input is 3.3V tolerant it does so with a clamp diode. A better solution would be to find a 3.3V bank as an input.
D	Driver on refdes U30-4 (pin name Y) has higher Vout Max (3.399000) than receiver Vin Max on refdes U1-AD40 (pin name DRAM_PWR_OK_C23)
13	The 74lvc1g125 can drive 3.3V. The processor input is max 1.5V. The circuit that is used (R353, R240) puts U30 in max current exceeding it's power limits.
D	Driver on refdes U57-T5 (pin name LASI_N_2) has lower Vout Max (1.8540) than receiver Vinh on refdes U49-C30 (pin name I_XLAUI_2_INT_N) (2.0) on
14	These pins are not defined as Open Drain. The output is 1.8V CMOS. The input is 3.3V CMOS
D	Driver on refdes U57-C5 (pin name LASI_N_0) has lower Vout Max (1.8540V) than receiver Vinh on refdes U49-AA25 (pin name I_XLAUI_0_INT_N)
15	These pins are not defined as Open Drain. The output is 1.8V CMOS. The input is 3.3V CMOS
D	Driver on refdes U18-6 (pin name O3) has higher Vol (0.55V) than receiver Vil on refdes U6 and U14 pins K4,G9,G18,K23 (pin names TCK[0:3]) (0.36V)
16	The M74LCX16244 is powered from 3.3V while the BCM84834 pin is powered from 2.5V
D	Driver on refdes U75-9 (pin name O5) has higher Vol (0.55V) than receiver Vil on refdes U4 and U12 pins L4,G8,G19,L23 (pin names TMS[0:3]) (0.36V) on
17	The M74LCX16244 is powered from 3.3V while the BCM84834 pin is powered from 2.5V

Warnings : 16

#	Defect Description Comments
W	Device U8's pin names do not agree with those specified in datasheet
1	Consider changing schematic symbol to agree with datasheet, in order to avoid downstream sustaining confusion.
W	Input pin K8 on refdes U45 has built in pull down. Please check that refdes R875 is sufficient to ensure proper thresholds
2	A 1K resistor may be more appropriate. (currently 10K)
W	Input pins L1,H2,H25,L26 on refdes U2 and U10 have built in pull down. Please check that refdes R2125 is sufficient to ensure proper thresholds
3	Because there are so many pins with built in pull down attached to R2125 it's probably a good idea to make it a smaller value to ensure that it's guaranteed
W	Input pin F4 on refdes U90 (on xxx) has built in pull down. Please check that refdes R14541 is sufficient to ensure proper thresholds
4	A 1K resistor should be used to ensure that minimum thresholds are obtained.
W	Input pin 2 on refdes U204 has built in pull up.
5	Please check that refdes R2799 is sufficient to ensure proper thresholds
W	10 instances of xxx FPGA (eg U20) talk to 20 instances of DRAM (eg U8). It is expected that DQab on one device should match with DQab on the other;
6	Suggestion is to re-align the DQ connections between xxx FPGAs and DRAMs such that DQxx matches on both sides. This will simplify debug and product
W	AMPC Flash U64 is a 16 bit device, attempting to talk to U65 (xxx CPLD) using a 32 bit address boundary via FLASHADDBUS_[2-27]
7	While this connection will work for functions such as lookups, it will not work for executable code. If that is required then FLASHADDBUS_1 needs to be
W	Differential input crosswired p -> n on net NP4-T41_XAUI2_CML_LANE28_MRB4_FC_N at U50-D23
8	Plus/minus swapped. No obvious reason for this.
W	Insufficient decoupling capacitance on net IWF N$114208 (on xxx) with 4 PWR pins and 0 capacitors
9	Suggest putting one more capacitor on this net.
W	Insufficient decoupling capacitance on net PCH_VCCSUS3P3_USB (on xxx) with 5 PWR pins and 0 capacitors
10	xxx pins AT8,AV11,AV12,AV9,BA12 connected to P3V3 via zero ohm R669 with no decoupling.
W	Insufficient decoupling capacitance on net IWF N$114208 (on xxx) with 4 PWR pins and 1 capacitors
11	Suggest putting one more capacitor on this net.
W	Input pin U35-22 tied directly to rail
12	Consider using a resistor to improve testability
W	Input pin U4-J11 tied directly to rail
13	Consider using a resistor to improve testability
W	U12 pin 4 and U118 pin G6 are power pins without decoupling capacitors
14	Consider addition of a 0.1uF ceramic capacitor at these pins
W	There are 3 resistors attached to net RTM_PRESENT_L. Please check intent. R144 (on xxx),R996 (on xxx),R1931 (on xxx),
15	Remove 2 resistors.
W	Devices U19,20 have pin # T4 defined as NC. Pin T4 does not exist and this should instead say Pin T7
16	Change Symbol to reflect pin T7 not T4